IN THE TITLE:

Please replace the title with the following replacement title.

PROCESSOR CONTROL APPARATUS FOR CONTROLLING ARITHMETIC UNITS, PROCESSOR AND PROCESSOR CONTROLLING METHOD

IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the last paragraph on page 22, with the following paragraph:

FIG. ~~10~~ 11 shows a block diagram showing an example of a processor comprising two arithmetic units and two instruction control units. In addition to the configuration according to the above-mentioned embodiment 1, the second arithmetic unit 14d comprises: a calculator 40 for performing an arithmetic operation; a first register file 41 for storing data (result of an arithmetic operation) generated by executing a series of instructions from the first instruction control unit 10d; a second register file 42 for storing data generated by executing a series of instructions from the second instruction control unit 11d; and an arithmetic unit selector 43 for switching data stored in either first register file 41 or second register file 42 according to an instruction from the second instruction decoder 33d, and providing the data for the calculator 40. For example, during the independent execution process of the second arithmetic unit 14d, an interrupt from the first instruction control unit 10d can be performed. FIG. 12 shows an example of a program containing a plurality of series of instructions stored in the first instruction memory (not shown in the drawings) and the second instruction memory 32d of the first instruction control unit 10d ~~oft he~~ of the processor shown in FIG. 11.

Please REPLACE the first paragraph on page 21, with the following paragraph:

FIG. 9 shows a block diagram showing an example of a processor comprising two arithmetic units 13c, 14c and two instruction control units. In addition to the configuration of the above-mentioned embodiment 1, the second instruction control unit 11c comprises an instruction queue 35 for temporarily storing series of instructions, an interrupt determination unit 36 for determining whether or not an interrupt can be performed during the execution of a series of instructions, and an AND circuit 37 for obtaining a logical product of the control signal output from the second instruction decoder 33c and the control signal output from the interrupt determination unit 36. The selector 34c switches depending on the output of the AND circuit 37 so that an interrupt can be performed from the first instruction control unit 10c during the independent execution process of the second arithmetic unit 14c. FIG. 10 shows an example of a program containing a plurality of instructions stored in the first instruction memory 30c and the second instruction memory 32c of the processor shown in FIG. 9.

Please REPLACE the second paragraph on page 26, with the following:

According to the present embodiment, the information as to which arithmetic unit drives each series of instructions of the series of time sharing instructions 52 is incorporated into the series of time sharing instructions 52 from the 0-th instruction control unit 50a. According to the information, the switch unit 53 issues a series of instructions in a time sharing manner (serially) to each instruction control unit. For example, if a series of instructions is to be issued to the first instruction control unit 10f, the switch unit 53 switches such that a series of instructions can be issued to the first instruction control unit 10f that includes a first instruction memory 30f. Upon receipt of the issued series of instructions, the first instruction control unit 10f switches the selector 34f, the first instruction decoder 31f decodes the series of instructions, and the first arithmetic unit 13f starts executing the series of instructions decoded by the first arithmetic unit 13f. When the series of time sharing instructions 52 issues a series of instructions, other instruction control units execute the process in a similar operation. Thus, arithmetic units are driven and operated in parallel by the series of time sharing instructions 52.

Please REPLACE the second paragraph on page 27, with the following:

FIG. 16 is a block diagram showing an example of a processor comprising two arithmetic units 13h, 14h and two instruction control units 10h, 11h with two instruction decoders 31h, 33h and a selector 34h. Each instruction control unit has common instruction memory 55, and does not have its own instruction memory. The instruction memory 55 has two ports (dual port), and issues from each port a series of instructions to an instruction decoder of each instruction control unit.

Please REPLACE the second paragraph on page 28, with the following:

FIG. 18 is a block diagram showing an example of the configuration of the processor whose electric power can be individually controlled by each instruction control unit 12i, and including a first through n-th arithmetic unit 13i, 15i. There are respective switches 56, 57 between the instruction control units other than the first instruction control unit 10i and corresponding arithmetic units. The power supply can be controlled by turning ON/OFF the switch according to a control signal from each instruction control unit based on the drive status of each arithmetic unit.